4/10/2000 0.43 Mt ENOW, 100 120 0200 TO, T 511 E15 0500 TMOB. 011 0E 015

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REMARKS

The abstract and summary have been amended as suggested by the examiner to satisfy the objections.

Claims 1 and 6 have been amended as suggested by the examiner to satisfy the objections.

Claims 1-10 have been amended to overcome the rejection under 35 U.S.C. § 103(a). Support for the amendment to Claims 1-10 may be found in the specification from page 11, line 14 to page 13, line 23.

Claims 1-10 are pending in the application.

By way of this response, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the examiner telephone Peter Scott at (719)533-7969 so that such issues may be resolved as expeditiously as possible.

Response to the rejection under 35 U.S.C. § 103

Claims 1 and 6 stand rejected under 35 U.S.C. §
103(a) as unpatentable over Morgan, U.S. Patent 6,530,073
(Morgan) in view of Tester, U.S. Patent 6,922,823 (Tester).
Applicant has amended Claims 1 and 6 to overcome the rejection as follows.

Claims 1 and 6 recite identifying and marking polygons in a generic data stream (GDSII) file in the integrated circuit design database to indicate a current state of the integrated circuit design database. In column 6, lines 52-62 cited by the rejection in section 7, page 3, Morgan teaches generating a gate level netlist generated from an RTL netlist. In contrast to Claims 1 and 6, Morgan does not teach

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or suggest identifying and marking polygons in a generic data stream file to indicate a current state of the integrated circuit design database. Further, in column 11, lines 40-50 cited by the rejection, Morgan teaches generating a list of changes to the gate level netlist, not identifying and marking polygons in the generic data stream file to distinguish objects included in the list of incremental changes that were changed from the current state. Also, Morgan teaches RTL annotation for changes to the gate level representation (see, for example, the title and column 6, lines 44-47), not identifying and marking polygons in a generic data stream file to distinguish polygons included in the list of incremental changes that were changed from the current state.

Because Morgan does not teach or suggest identifying or marking polygons in a generic data stream file to indicate a current state of the integrated circuit design database, and because Morgan does not teach or suggest identifying or marking polygons in the generic data stream file to distinguish polygons included in the list of incremental changes that were changed from the current state, Claims 1 and 6 are not obvious under 35 U.S.C. § 103(a).

The rejection of Claims 2-5 and 7-10 is traversed for the same reasons explained above.

Applicant respectfully requests examination and favorable reconsideration of Claims 1-10.

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No additional fee is believed due for this amendment.

Respectfully submitted,
/ Eric James Whitesell /
Eric James Whitesell #38657

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